

FIG. 1 is a block diagram of a data processing system 100. The system 100 includes a plurality of processing units 102, each of which includes a D-type flip-flop (D1) and an output register (OUT). The D1 flip-flop is connected to an input (IN) and an output (OUT). The output register (OUT) is connected to the output of the D1 flip-flop. The system 100 also includes a plurality of control signals, including a clock signal (Φ1) and a data signal (Φ2). The clock signal (Φ1) is connected to the clock input of the D1 flip-flop. The data signal (Φ2) is connected to the data input of the D1 flip-flop. The system 100 further includes a plurality of control signals, including a clock signal (Φ1) and a data signal (Φ2). The clock signal (Φ1) is connected to the clock input of the D1 flip-flop. The data signal (Φ2) is connected to the data input of the D1 flip-flop.

100

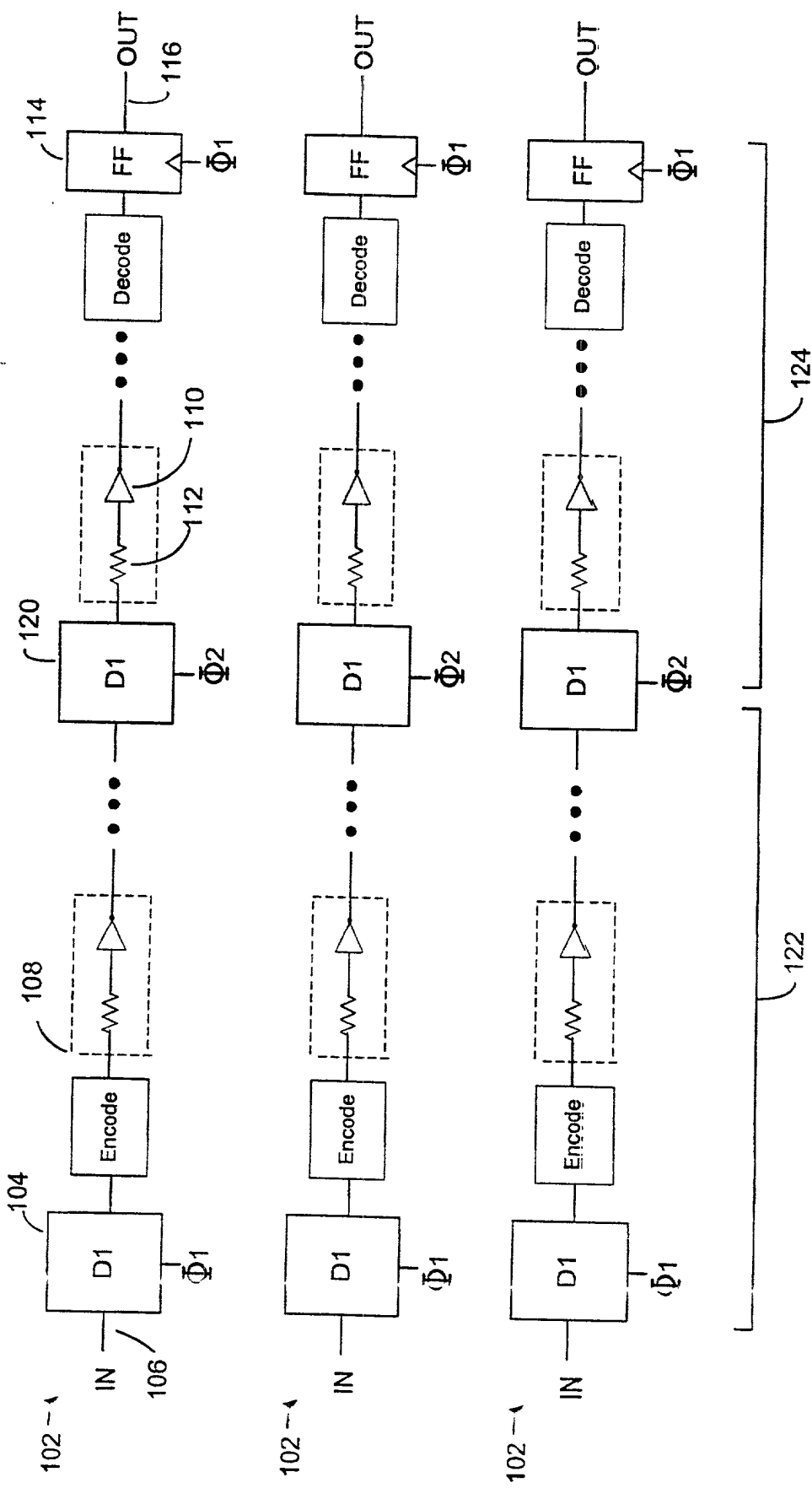


FIG. 1

200 ↗

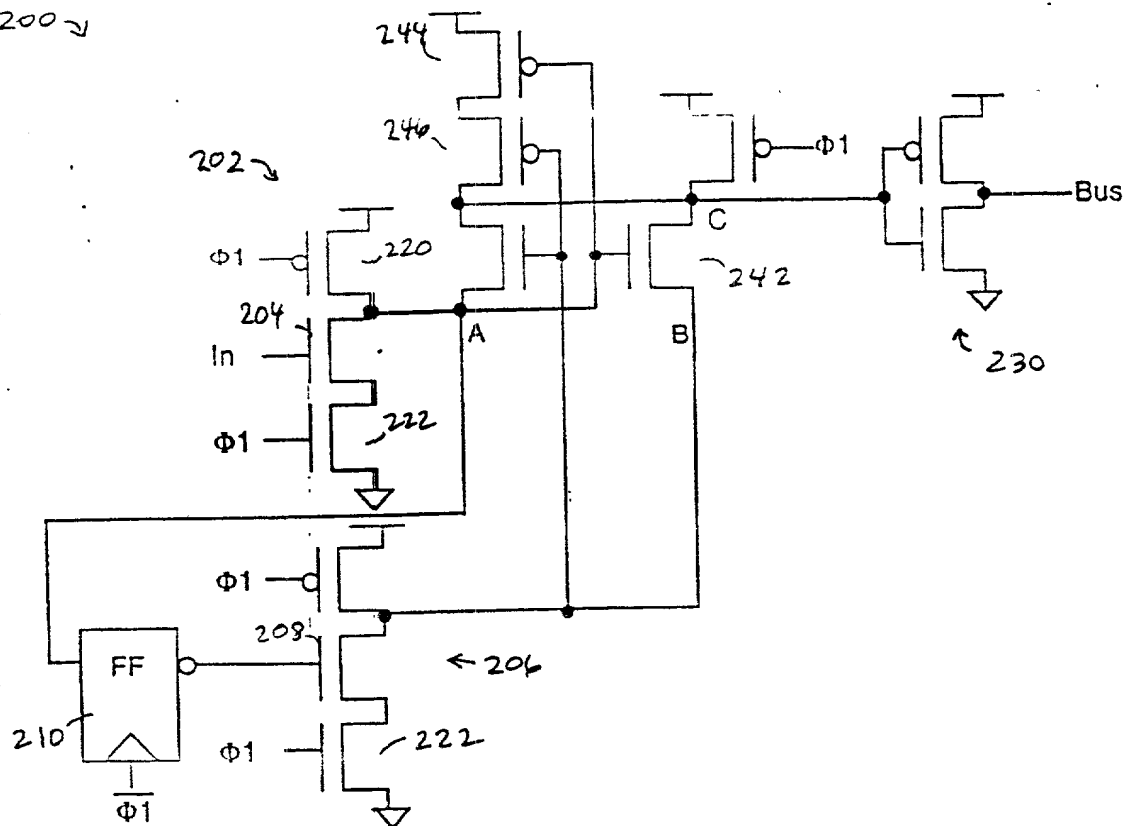


FIG. 2

300 ↗

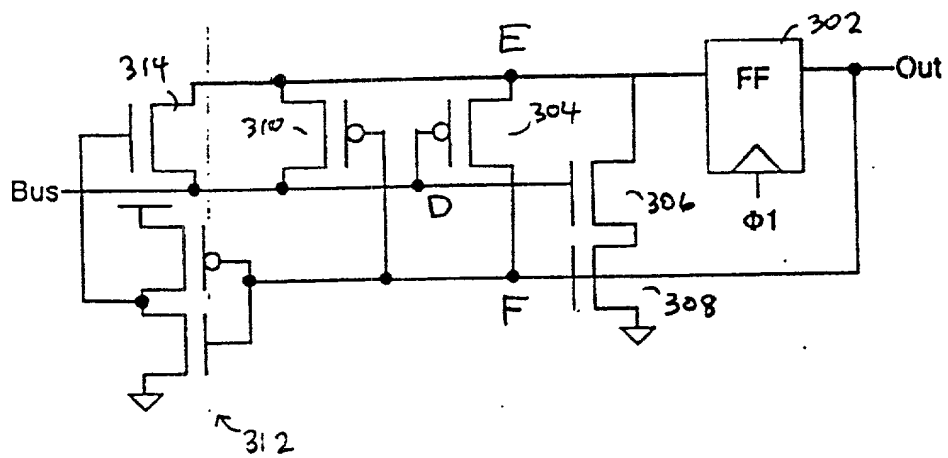


FIG. 3